REMARKS

This paper is submitted in reply to the Office Action dated March 22, 2007, within the three-month period for response. Reconsideration and allowance of all pending claims are respectfully requested.

In the subject Office Action, claims 1-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6070,009 to Dean et al. (hereinafter "Dean").

Applicant respectfully traverses the Examiner's rejections to the extent that they are maintained. Applicant has canceled claims 3-5, 7, 19-21 and 31 and amended claims 1, 6, 8, 10, 17, 22, 24 and 30, and Applicant submits that no new matter is being added by the above amendments, as the amendments are fully supported in the specification, drawings and claims as originally filed. Applicant also notes that the amendments made herein are being made only for facilitating expeditious prosecution of the aforementioned claimed subject matter. Applicant is not conceding in this application that the originally-claimed subject matter is not patentable over the art cited by the Examiner, and Applicant respectfully reserves the right to pursue this and other subject matter in one or more continuation and/or divisional patent applications.

As an initial matter, Applicant wishes to thank the Examiner for the consideration granted in the telephone interview conducted with the undersigned on June 21, 2007. In the interview, Applicant proposed amendments to claim 1 to address the Examiner's rejections, as well as discussed distinctions between the claimed invention and Dean. Applicant also requested the Examiner provide a PTO-892 form to Applicant citing Dean. The Examiner did indicate that additional language in claim 1 overcame Dean, but that further searching would be required prior to allowance. The Examiner also agreed to contact the undersigned should the Examiner require any additional amendments in order to pass the case to allowance. Applicant urges the Examiner to contact the undersigned at 513-241-2324 should there be any outstanding issues that remain to be resolved prior to allowing the Application.

Now turning to the subject Office Action, and initially to §101 issues, in view of the Examiner's comments with respect to §101, Applicant has elected to amend

claim 30 to recite a "recordable" medium, and has canceled claim 31 accordingly. As discussed at page 10, line 23 to page 11, line 3, recordable type media are specifically defined as including various physical media, and furthermore, recordable type media are explicitly distinguished in the specification from signals, and in particular "transmission type media." While Applicant is of the belief that claim 30 in its original form was in compliance with §101, Applicant nonetheless submits that as amended the claim now comports with the Office's current interpretation of the statute.

Next, turning to art-based rejections, and specifically to the rejection of claim 1, this claim generally recites a method of ordering program code in a computer memory. The method includes selecting an ordering from among a plurality of orderings for a plurality of program code segments using a heuristic algorithm, and ordering the plurality of program code segments in a memory of a computer using the selected ordering.

Claim 1 has been amended herein to incorporate the subject matter of claim 7, and now additionally recites that the heuristic algorithm comprises a simulated annealing algorithm, that selecting the ordering using the heuristic algorithm includes testing a subset of the plurality of orderings, and that testing the subset of the plurality of orderings includes, for each ordering in the subset, calculating a cost for such ordering based upon cache miss rates for such ordering, and randomly selecting a different ordering after testing an ordering from the subset of orderings. Claims 3-5 and 7 have been canceled, and claims 6, 8 and 10 amended, for consistency with the amendments made to claim 1.

As Applicant discussed in the interview, Dean does not disclose the use of a heuristic algorithm to select from among a plurality of orderings for program code segments, or ordering the program segments in a computer memory using a selected ordering. The Examiner cites col. 22 of Dean; however, the only reference to heuristics in this passage relates to heuristic mechanisms in processors that control out-of-order instruction execution and memory operations (see, in particular, col. 22, lines 28-34). The heuristics therefore relate to the operation of a processor that executes a program, and not to any ordering of program code in a memory.

Furthermore, with respect to claim 7, the subject matter of which has now been incorporated into claim 1, the Examiner relies on col. 24, lines 1-10 along with col. 22. Col. 24, however, discusses "randomness" only in connection with the selection of instructions to sample. The passage is not relevant to any random selection of orderings of program code segments.

Claim 1 as amended focuses on the use of a heuristic simulated annealing algorithm that tests different orderings of program code segments in a memory by calculating a cost for different potential orderings based upon cache miss rates for such orderings, and randomly selecting a different ordering after a particular ordering has been tested. The purpose of the invention recited in claim 1 is to minimize the frequency of cache misses that occur when fetching instructions in a program. Of note, the cache misses of interest are not cache misses due to the fetching of data by program instructions. Instead, the cache misses of interest are due to the execution of program instructions themselves, i.e., the retrieval of instructions rather than the retrieval of data under the command of instructions.

Dean, in contrast, is directed to randomly sampling instructions executing in a program to profile the program, potentially for the purpose of determining how to optimize the program. As the Examiner acknowledged in the interview, Dean is focused upon execution paths and path profiles, but not on the ordering of program code segments in a memory to minimize cache misses. Furthermore, Dean does not attempt to calculate costs for program code orderings, nor does Dean randomly select different orderings of program code segments, as is also required by claim 1.

Applicant can find no disclosure or suggestion in Dean of any mechanism for using a simulated annealing algorithm to select from among a plurality of different potential orderings of program code segments. Dean also does not disclose or suggest calculating a cost for a particular ordering based upon the cache miss rate for the ordering. Dean additionally does not disclose or suggest randomly selecting a different ordering of program code segments after another ordering has been tested. Absent any disclosure of such concepts, Dean cannot be relied upon to anticipate claim 1, and withdrawal of the rejection of claim 1 is therefore respectfully requested.

In addition, claim 1 is non-obvious over Dean as there is no suggestion in the reference of the desirability of using a simulated annealing algorithm to select from among different orderings of program code segments, where that algorithm calculates relative costs based upon cache miss rates, and where the algorithm utilizes randomness to select which orderings to test. Absent any such suggestion, claim 1 is non-obvious over Dean. Reconsideration and allowance of claim 1, and of claims 2, 6, and 8-16 are therefore respectfully requested.

Next, with respect to the rejections of independent claims 17 and 30, each of these claims has been amended in a similar manner to claim 1, and now recites in part that the heuristic algorithm comprises a simulated annealing algorithm, that the first program code is configured to select the ordering using the heuristic algorithm by testing a subset of the plurality of orderings, that the first program code is configured to test the subset of the plurality of orderings by, for each ordering in the subset, calculating a cost for such ordering based upon cache miss rates for such ordering, and that the first program code is configured to test the subset of orderings by randomly selecting a different ordering after testing an ordering from the subset of orderings. Claims 19-21 have been canceled, and claims 22 and 24 have been amended, for consistency with the amendments to claims 17 and 30.

As discussed above in connection with claim 1, the aforementioned combination of features is not disclosed or suggested by Dean. Independent claims 17 and 30 are therefore novel and non-obvious for the same reasons as presented above for claim 1. Reconsideration and allowance of independent claims 17 and 30, and of claims 18 and 22-29 which depend therefrom, are therefore respectfully requested.

Finally, Applicant traverses the Examiner's rejections of the dependent claims based upon their dependency on the aforementioned independent claims. Nonetheless, Applicant does note that a number of these claims recite additional features that further distinguish these claims from the references cited by the Examiner. For example, claims 8 and 22 recite that the random selection of a different ordering includes the swapping of two program code segments in a previous ordering. The Examiner cites col. 23, line 7 to col.

24, line 10 of Dean; however, the cited passage is focused upon hot and cold paths, and analyzing branch histories and control flow graphs. There is nothing in the cited passage directed to swapping program code segments in an ordering of program code for the purpose of minimizing cache misses arising from the fetching of the instructions in the program code segments, and as such, Dean fails to anticipate this feature of claims 8 and 22.

Also, claims 9 and 23 recite that the program code segments each comprise a module, and that the random selection of the different ordering further comprises constraining selection of the two program code segments to modules in the same replaceable unit destination. In rejecting these claims the Examiner relies on cols. 23 and 24 of Dean; however, Applicant can find no discussion of constraining the ordering of modules to a replaceable unit destination in the cited passage. As such, Applicant submits the Examiner has not met the burden necessary to establish anticipation of these claims by Dean.

In addition, claims 13 and 26 recite that selecting an ordering from among the plurality of orderings further comprises randomly accepting a change to an ordering even if the calculated cost for such ordering is not lower than that of the working ordering. In rejecting these claims, the Examiner cites col. 24, lines 55-67. The cited passage, however, merely discloses shifting bits in a shift register, and appears to have no relevance to randomly accepting changes to an ordering of program code segments, particularly when such changes result in a cost that is not lower than that of a working ordering. Again, Applicant submits the Examiner has not met the burden necessary to establish anticipation of these claims by Dean.

In summary, Applicant respectfully submits that all pending claims are novel and non-obvious over the prior art of record. Reconsideration and allowance of all pending claims are therefore respectfully requested. If the Examiner has any questions regarding the foregoing, or which might otherwise further this case onto allowance, the Examiner may contact the undersigned at (513) 241-2324. Moreover, if any other charges or credits

are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,

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Date

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